Smart ATE PCB Routing System An Innovative Solution for Accelerating PCB Design

Ms. B. Lokapriya
IC Test Engineer

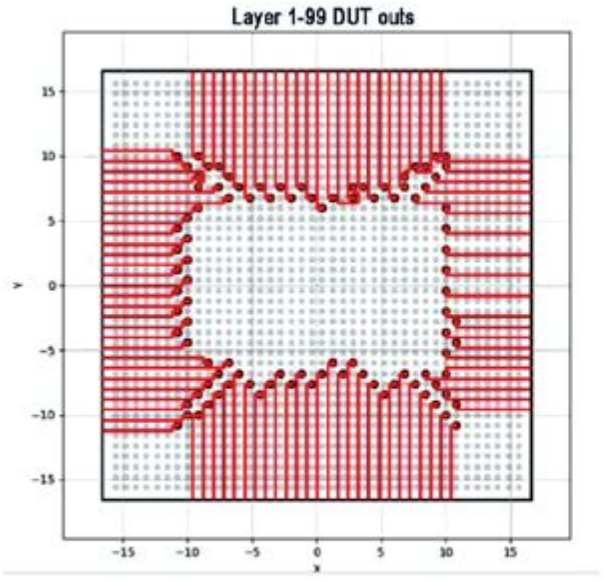
Caliber Interconnects Pvt. Ltd., a prominent leader in semiconductor design and test engineering, introduces the Smart ATE PCB Routing System, a breakthrough innovation that transforms traditional ATE board design. Powered by our custom RouteIQ Engine, integrated with the Hungarian Algorithm, the system delivers a structured multi-stage work flow encompassing signal planning, layer optimization, and tester channel mapping enabling intelligent, highly efficient ATE PCB routing.

The conventional development cycle of Automated Test Equipment (ATE) interface PCBs is highly dependent on manual processes, particularly during the critical stages of signal layer planning and tester channel assignment.

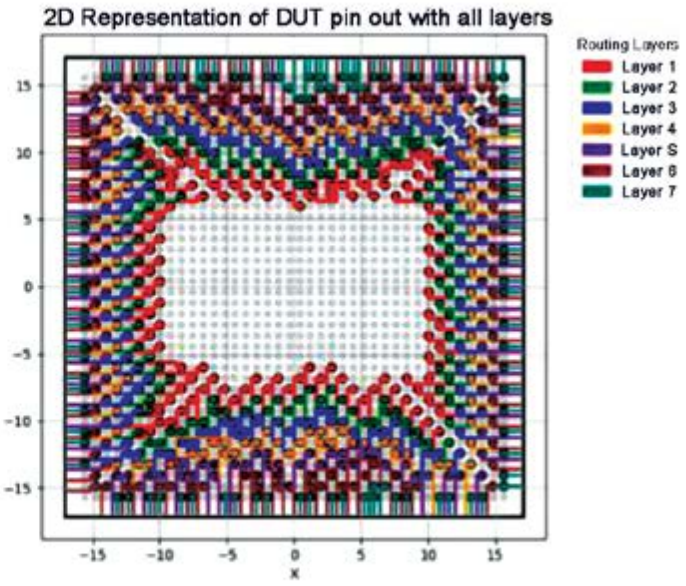
- Time-consuming & error-prone
- Complex constraint management
- Poor optimization
- Reduced efficiency
- Lack of automation

Modern EDA tools simplify schematic and layout design but still lack automation for signal layer planning and tester channel assignment both essential pre-routing steps in ATE interface board development. This work introduces a smart automation framework that performs these tasks with minimal user input while complying with constraints such as anti-pad spacing, routing boundaries, and signal-integrity requirements. The underlying algorithm operates in a structured, constraint-aware manner, systematically planning DUT signal escapes and assigning tester channels to achieve optimal trace utilization and minimal layer count.

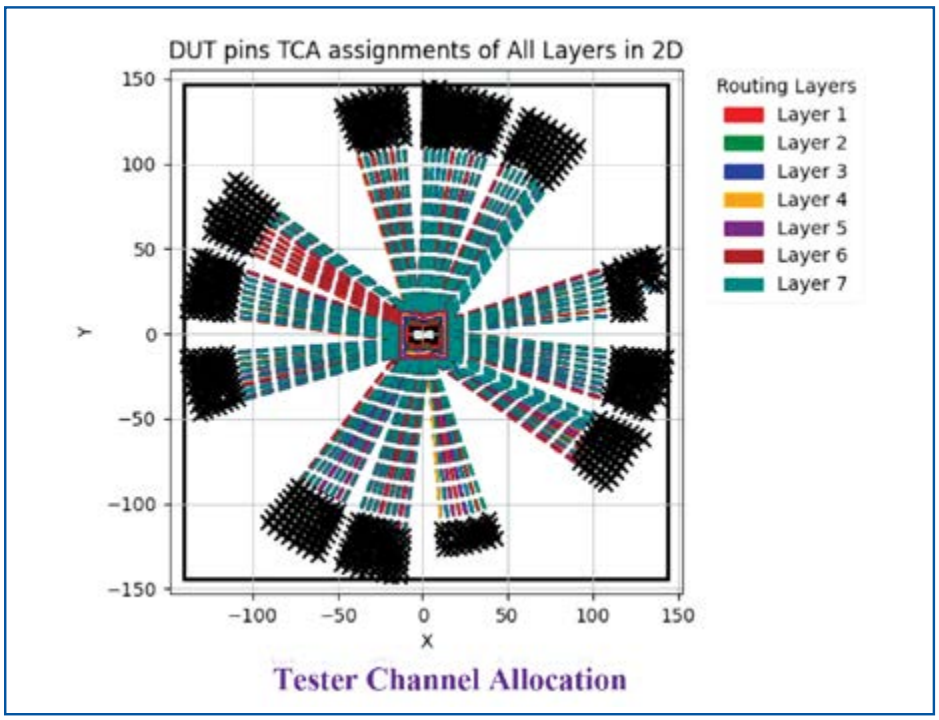
The work flow begins with input pre-processing, mapping DUT pin coordinates, signal pin locations, tester channel positions, and the BGA outline. Signal pins are then



DUT Out

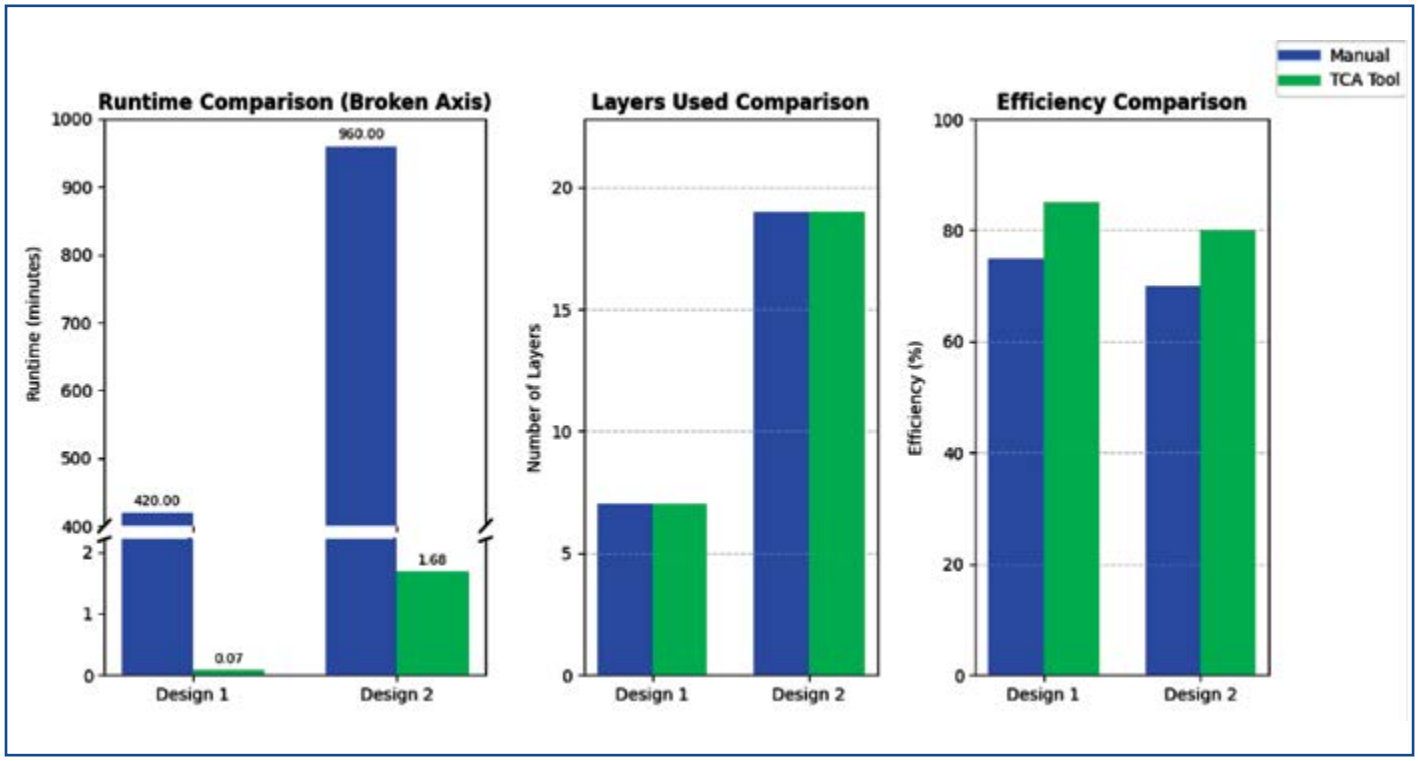


Layer Allocation



Tester Channel Allocation

Mr. A. Dyaneswaran
IC Test Engineer



reordered in a spiral pattern from the center outward to ensure efficient routing. Each pin undergoes directional path finding to determine a valid DUT escape point while honoring spatial constraints. Routing is performed layer by layer using a dynamic allocation strategy to maintain isolation and minimize crosstalk. After DUT-out planning, tester channel assignment is carried out using the Hungarian Algorithm to achieve an optimal, low-cost mapping of channels to signals.

The tool generates a structured output that includes comprehensive routing and assignment data. This output features a layer-wise signal pin mapping, listing the pins routed per layer along with corresponding trace length statistics. It also provides visual layer maps, where routed paths are displayed using layer-specific color coding to facilitate quick verification. Additionally, a tester channel assignment table is generated, correlating each signal pin with its mapped tester channel. An unrouted pin report is also included, identifying pins that could not be routed due to spatial violations or tester constraints, enabling further analysis and manual intervention if necessary.

The proposed smart methodology significantly reduces dependency on manual judgement and experience by introducing algorithm-driven planning that enhances both speed and reliability. Accuracy is improved through algorithmic checks that eliminate overlaps and prevent violations of electrical constrains. The methodology also optimizes layer usage by maximizing signal escape per layer, thereby minimizing the total number of layers required. Additionally, it ensures predictable signal integrity by maintaining uniform routing lengths and spacing, which contributes to consistent and reliable signal performance across all channels.

The proposed automated methodology lays a strong foundation for accelerating ATE interface PCB development, with several strategic enhancements planned. Caliber's future improvements include support for non-standard BGA layouts, on-layout routing visualization with automated ART file generation, and impedance-driven trace-width calculation. Integrated stack-up estimation will determine the optimal layer count based on signal density, impedance needs, and isolation constraints. Advanced capabilities such as delay tuning and differential-pair management will further enhance performance. Collectively, these upgrades aim to deliver a fully intelligent design assistant that seamlessly bridges logical planning and physical realization, reducing design iterations and ensuring robust, production-ready ATE hardware.

We're delighted to share that our paper "Accelerating Time to Market of Semiconductor ICs Using Smart ATE PCB Routing System" was presented at the IEEE 9th International Test Conference India (ITC India 2025) and later published in IEEE (September 2025) authored by Lokapriya B, Dyaneswaran A, Karthika R, Lokendran S, and Senthil Kumar Dhamodharan of Caliber Interconnects.